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TECHNICAL REPORT

Radiation Effects in III-V Nanowire Devices

September 2016

HDTRA1-11-1-0021

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14. ABSTRACT

The top-down fabrication of an in-plane nanowire (NW) GaAs metal-oxide-semiconductor field-effect transistor (MOSFET) by focused-ion beam (FIB) etching and chemical oxidation is reported. The device has a semiconductor-on-insulator structure with an n+-GaAs/Al2O3 layer stack implemented by lateral hydrolyzation oxidation. A 2 micron-long channel having an effective cross section ~70 x 220 nm is directly fabricated into the n+-GaAs layer by FIB etching. The channel is electronically isolated from the substrate by the Al2O3 layer and is effectively an in-plane NW epitaxially connected to the source and drain for a planar MOSFET within a single layer. The NW channel is surrounded by an ~15 nm-thick gate oxide.

15. SUBJECT TERMS

in-plane nanowires, III-V MOSFET, lateral oxidation, FIB etching

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UNIT CONVERSION TABLE

U.S. customary units to and from international units of measurement*

U.S. Customary Units	Multiply by → / ← Divide by†		International Units
Length/Area/Volume			
inch (in)	2.54	$\times 10^{-2}$	meter (m)
foot (ft)	3.048	$\times 10^{-1}$	meter (m)
yard (yd)	9.144	$\times 10^{-1}$	meter (m)
mile (mi, international)	1.609 344	$\times 10^{3}$	meter (m)
mile (nmi, nautical, U.S.)	1.852	$\times 10^{3}$	meter (m)
barn (b)	1	$\times 10^{-28}$	square meter (m^2)
gallon (gal, U.S. liquid)	3.785 412	$\times 10^{-3}$	cubic meter (m^3)
cubic foot (ft^3)	2.831 685	$\times 10^{-2}$	cubic meter (m^3)
Mass/Density			
pound (lb)	4.535 924	$\times 10^{-1}$	kilogram (kg)
unified atomic mass unit (amu)	1.660 539	$\times 10^{-27}$	kilogram (kg)
pound-mass per cubic foot (lb ft^{-3})	1.601 846	$\times 10^{1}$	kilogram per cubic meter (kg m^{-3})
pound-force (lbf avoirdupois)	4.448 222		newton (N)
Energy/Work/Power			
electron volt (eV)	1.602 177	$\times 10^{-19}$	joule (J)
erg	1	$\times 10^{-7}$	joule (J)
kiloton (kt) (TNT equivalent)	4.184	$\times 10^{12}$	joule (J)
British thermal unit (Btu) (thermochemical)	1.054 350	$\times 10^{3}$	joule (J)
foot-pound-force (ft lbf)	1.355 818		joule (J)
calorie (cal) (thermochemical)	4.184		joule (J)
Pressure			
atmosphere (atm)	1.013 250	$\times 10^{5}$	pascal (Pa)
pound force per square inch (psi)	6.984 757	$\times 10^{3}$	pascal (Pa)
Temperature			
degree Fahrenheit (^oF)	$[T(^oF) - 32]/1.8$		degree Celsius (^oC)
degree Fahrenheit (^oF)	$[T(^oF) + 459.67]/1.8$		kelvin (K)
Radiation			
curie (Ci) [activity of radionuclides]	3.7	$\times 10^{10}$	per second (s^{-1}) [becquerel (Bq)]
roentgen (R) [air exposure]	2.579 760	$\times 10^{-4}$	coulomb per kilogram (C kg^{-1})
rad [absorbed dose]	1	$\times 10^{-2}$	joule per kilogram (J kg^{-1}) [gray (Gy)]
rem [equivalent and effective dose]	1	$\times 10^{-2}$	joule per kilogram (J kg^{-1}) [sievert (Sv)]

*Specific details regarding the implementation of SI units may be viewed at http://www.bipm.org/en/si/.

†Multiply the U.S. customary unit by the factor to get the international unit. Divide the international unit by the factor to get the U.S. customary unit.

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What are the major goals of the project?

List the major goals of the project as stated in the approved application or as approved by the agency. If the application lists milestones/target dates for important activities or phases of the project, identify these dates and show actual completion dates or the percentage of completion. Generally, the goals will not change from one reporting period to the next. However, if the awarding agency approved changes to the goals during the reporting period, list the revised goals and objectives. Also explain any significant changes in approach or methods from the agency approved application or plan.

The objectives of this program were to: *a*) develop a new nanowire transistor technology based on nanoscale lithography and III-V nanoepitaxial growth that provides in-plane nanowires with integrated contacts and is scalable to large numbers and high densities of nanowires; and *b*) to investigate the impact of energetic radiation on these intrinsically radiation resistant (nanoscale devices and radiation resistant materials), innovative devices. (unchanged from proposal)

What was accomplished under these goals?
For this reporting period describe: 1) major activities; 2) specific objectives; 3) significant results, including major findings, developments, or conclusions (both positive and negative); and 4) key outcomes or other achievements. Include a discussion of stated goals not met. As the project progresses, the emphasis in reporting in this section should shift from reporting activities to reporting accomplishments.

Progress has been made in a number of areas during this program. These include:

- Final mask layout for minimal lateral wet oxidation
- Fabrication of ~70 nm-wide in-plane GaAs nanowire arrays by interferometric lithography and plasma etching
- Electrical characterization of in-plane nanowire GaAs FETs
- Epitaxial growth of InAs nanowires for FET applications

Details are provided below.

Introduction

Nanowires are a potential structure for replacing planar CMOS in next generation electronics. Most investigations have relied on vertical growth (often with wire-to-wire variations in linewidths and random positioning) based on vapor-liquid-solid (VLS) catalyzed growth. Moving this technology from single transistor measurements to the construction of circuits with billions of transistors to complement existing integrated circuit technologies would require pick and place technologies to which are inherently slow and non-scalable. An attractive alternative that has received much less attention is the top-down fabrication of in-plane nanowires where the relative locations and interconnections are defined by lithographic processes. We are exploring the capabilities of III-V semiconductors in a SOI geometry which are well-developed technologies capability of scaling to dense circuit structures with the inherent radiation hardness of III-V materials and the additional advantage of very small and thin structures.

The overall outline of the process includes:

- epitaxial growth of a multilayer III-V stack including a sacrificial AlGaAs layer that will be oxidized to provide the isolation from the substrate.
- local area growth of a nanowire or top-down definition of a nanowire by lithographic processes (FIB to date).
- removal of the oxidized AlGaAs layer under the nanowire.
- oxidation of the nanowire to provide the gate isolation.
- fabrication of gate and source/drain contacts
- electrical characterization of the fabricated transistor.

We have finalized the mask layout for the lateral wet oxidation (LWO) adequate to the fabrication of sub-100 nm-wide GaAs in-plane (IP) nanowires (NWs), based on the results of the last year. We have fabricated an array of GaAs IPNWs with channel widths reduced to ~70 nm with interferometric lithography (IL) and plasma etching. The electrical characteristics have been reported. To resolve the limitation on the top-down process in the NW uniformity along the channel, we have investigated InAs NWs epitaxially grown on a nonplanar Si(001) substrate.

Final layout for sub-100 nm-wide in-plane NWs

The unique characteristics of our FETs are the SOI structure by LWO for an in-plane nanowire that is physically connected to the substrate but electronically isolated from it and the fabrication of an entire NW FET including ohmic source/drain contacts prepared in a single layer. This approach resolves the issues of the difficulties in gate fabrication on a vertical NW and the contact resistance in the metalization to the NW. However, this FET requires a finite LWO area for the whole device that is considerably larger than that for the NWs alone. Previously, we demonstrated the reduction of the area of LWO for a single device that dramatically increased the yield of ~200 nm-wide GaAs channel FET process. Figure 1(a) shows a device pattern similar to the layout used at the end of this program. In some cases of the devices fabricated with this layout particularly the device for sub-100 nm channels, however, the degradation of the devices by LWO such as peel-off or delamination of the NWs from a substrate is still observed along the periphery of a trench fabricated for hot water vapor to access the $Al_{0.98}Ga_{0.02}As$ layer laterally. The trench is indicated with a red dashed box in Fig. 1(a). We found that this layout worked at the scale above 100 nm but was not adequate to the NWs at the sub-100nm scale. To resolve this issue, the device layout were revised to Fig. 1(b), where the area and periphery for trench opening is reduced from 75×10 μm^2 and 170 μm in Fig. 1(a) to 15×10 μm^2 and 50 μm. The NW array will be fabricated in the dashed box in Fig. 1(b). LWO proceeds uniformly from the trench periphery and the oxidized area by LWO is roughly proportional to the length of the periphery. The pattern in Fig. 1(b) for a single FET has the least LWO area for an entire device including contact pads that corresponds to ~60 % of the LWO area from the pattern in Fig. 1(a). As seen later, the FETs fabricated with the layout in Fig. 1(b) shows negligible delamination for sub-100 nm IPNW FETs after LWO.

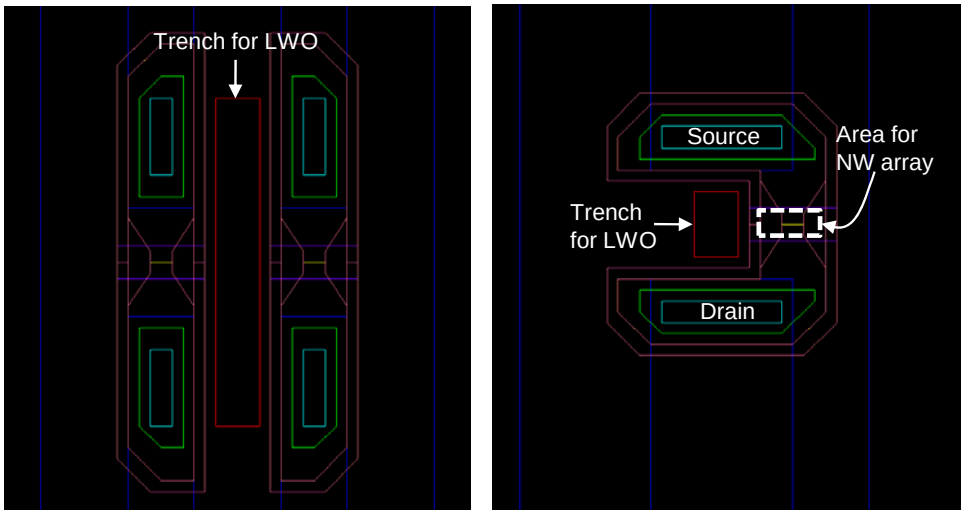


Figure 1 (a) FET layout used in the last year. (b) A layout of FET revised for sub-100 nm NW channel array. In (b), the dashed box indicates the area for NW array.

Fabrication of ~70 nm-wide GaAs NW arrays by IL

With *i*-line IL and chlorine-based plasma etching, sub-100 nm in-plane GaAs NW arrays have been fabricated. Most of the fabrication process is similar to that reported last year except for the last few steps which were revised for IL. Since IL is a lithography technique for nonselective exposure, an additional photomask was required to confine a one-dimensional interference pattern from IL to a channel area indicated in Fig. 1(b). Since the period of the array is set to 500 nm, precise alignment of the μm-scale photomask to the one-dimensional (1D) interference pattern to save all NWs under the photomask is not available. As seen later, this causes the photomask to block the patterns for the NWs located at both side ends of a given array incompletely. However, the NWs improperly fabricated near the edge are typically narrower and poorer than others in the inner side of the array in width and uniformity, and do not contribute significantly to electrical conduction through the NW array and will not be considered in further analysis.

Figure 2(a) shows a layer structure used for device fabrication that was grown by molecular beam epitaxy (MBE). Compared with the layer structure used last year, the n^+-GaAs layer at the top for the device is increased from 100 to 150 nm and the $Al_{0.98}Ga_{0.02}As$ layer for SOI by LWO is reduced from 500 nm to 300 nm in thickness. The thickness change of the n^+-GaAs layer was to allow for the unexpected vertical oxidation proceeding upward from the n^+-GaAs/$Al_{0.98}Ga_{0.02}As$ interface into the n^+-GaAs layer that results in the reduction of the effective n^+-GaAs layer thickness that was discovered last year and to enhance fin FET effects. The actual thickness of the n^+-GaAs layer after LWO would be reduced to ~130 nm by the vertical oxidation of GaAs. The change in the $Al_{0.98}Ga_{0.02}As$ layer is for further relief of the stress effects by the volume shrinkage from LWO under the thicker n^+-GaAs layer.

Figures 3(a) and 3(b) are scanning electron microscopy (SEM) images of the devices fabricated with the layout shown in Figs. 1(a) and 1(b) before the fabrication of gate metal and contact pads, respectively. The oxidation time was not very different from that used in the last year (~10 minutes) but, as explained earlier, the periphery of the trench of Fig. 3(b) is significantly reduced and most of the devices (~100 %) survived by visual inspection after LWO while those similar to Fig. 3(a) exhibit ~80% survival. Thus, the delamination issue from LWO for sub-100nm IPNWs has been resolved with the device pattern in Fig. 1(b).

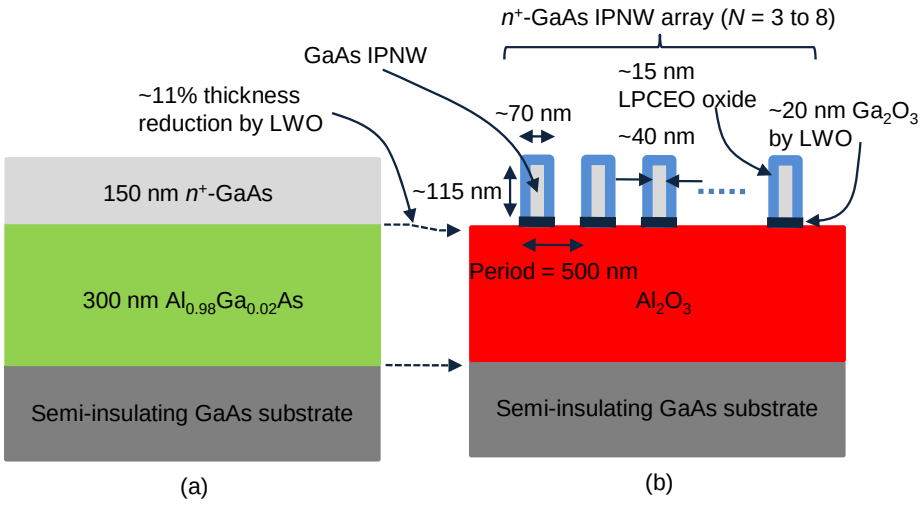


Figure 2 (a) The layer structure used for IPNW FET. (b) A cross section of an IPNW array FET . In (b), *N* means the number of IPNWs in an array that ranges from 3 to 8. The period of the array is 500 nm. The effective channel cross area after LWO and LPCEO is reduced to ~40 nm × 115 nm from the original area of 70 nm × 150 nm. Each NW is covered by LPCEO oxide and Ga_2O_3 from LWO that play a role of gate oxide.

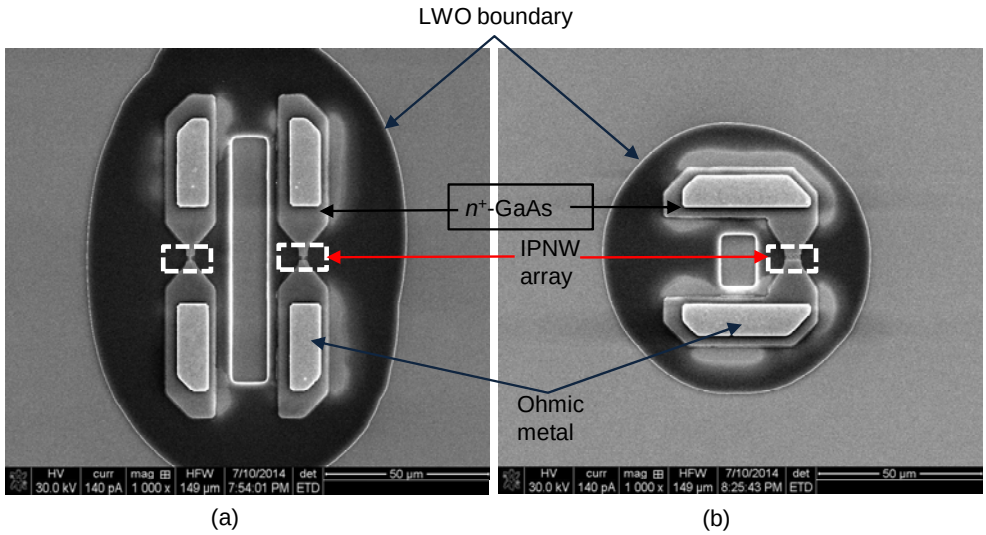


Figure 3 Top-down SEM images of IPNW FET fabricated with (a) the layout in Fig. 1(a) and (b) the layout in Fig. 1(b). The area inside the LWO boundary [a black oval in (a) and a black circle in (b)] are Al_2O_3 and the devices are fabricated on it.

In Fig. 3, the boundary of the oxidized $Al_{0.98}Ga_{0.02}As$ layer or the Al_2O_y (y ~ 3) layer was clearly revealed by plasma etching, as indicated by an arrow in each device. This is because Al_2O_y has considerably low etch rate compared with $Al_{0.98}Ga_{0.02}As$. Such different etch rates positively contribute to electrical device isolation from the remaining area. Figure 4 is SEM images of the channel arrays fabricated at the middle of the devices by IL and plasma etching.

The period of the array pattern projected on the photoresist film was set to 500 nm by IL. The length of the channel is ~2 μm. The number of the NWs in the array, *N*, is 3 in Fig. 4(a) and 7 in Fig. 4(b). Figure 4(b) is the enlargement of the dashed box in Fig. 3(b). As mentioned above, the NWs at the side edge were partially removed as a result of misalignment of the photomask to the device beyond control limit of our present photolithography, and not counted. The plasma etching to transfer the PR pattern to the n^+-GaAs layer was performed so that it completely removed the n^+-GaAs layer between NWs. The width of individual NWs are roughly in the range of 60 - 80 nm. In most NWs, the narrowest width is achieved at the middle of them because of the second UV exposure with a μm-scale photomask to confine the IL pattern onto the channel region. The resulting cross section of the array along the dotted line in Fig. 4(b) is schematically illustrated in Fig. 2(b) with scale close to actual physical dimensions of the NWs. In the consideration of the aspect ratio of the NWs, the array period ~ 500 nm is wide enough for the access of chemicals in LPCEO and the conformal deposition of gate metal by electron-beam evaporation.

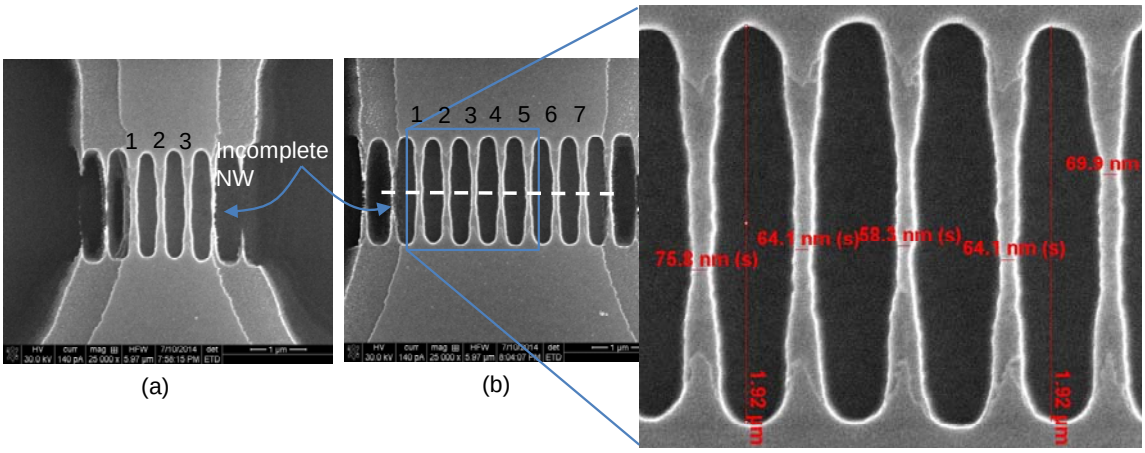


Figure 4 Top-down SEM images of IPNW arrays with (a) $N = 3$ and (b) $N = 7$, as denoted by the numbers labeling NWs in each figure. The incomplete NW at both sides were not counted, as explained in the text. The dashed box in Fig. 3(b) corresponds to (b). The cross section along the dashed line in (b) corresponds to Fig. 2(b). The enlargement in (b) presents the scale of individual NWs. The channel length is ~ 2 μm.

Characterization of GaAs oxide by LPCEO

The roughness of the oxidation front (the boundary between oxidized and unoxidized GaAs) in LPCEO is important for the current passing through a NW channel of which the surface is oxidized by LPCEO for gate oxide because it is related to the surface scattering of electrons. For the relation of surface morphology to oxide thickness (or oxidation time), the surface morphology of the oxide layer was examined with the variation of oxidation time or oxide thickness. Figure 5(a) shows plan view (top down) SEM images from planar n^+-GaAs without LPCEO on the left, with 5 min LPCEO in the middle, and 55 min LPCEO on the right. The scale bar in the right bottom in each image is 500 nm. A 5 min. LPCEO corresponds to about 15 nm-thick oxide and 55 min oxidation results in ~100 nm-thick oxide on the channel. It is clear that the surface morphology is degraded as oxidation time increases. Degradation of surface morphology is evident for 55 min but is not so much for 5 min etching. This means

LPCEO may not be a good for thick oxide but is acceptable for thin oxide in surface morphology.

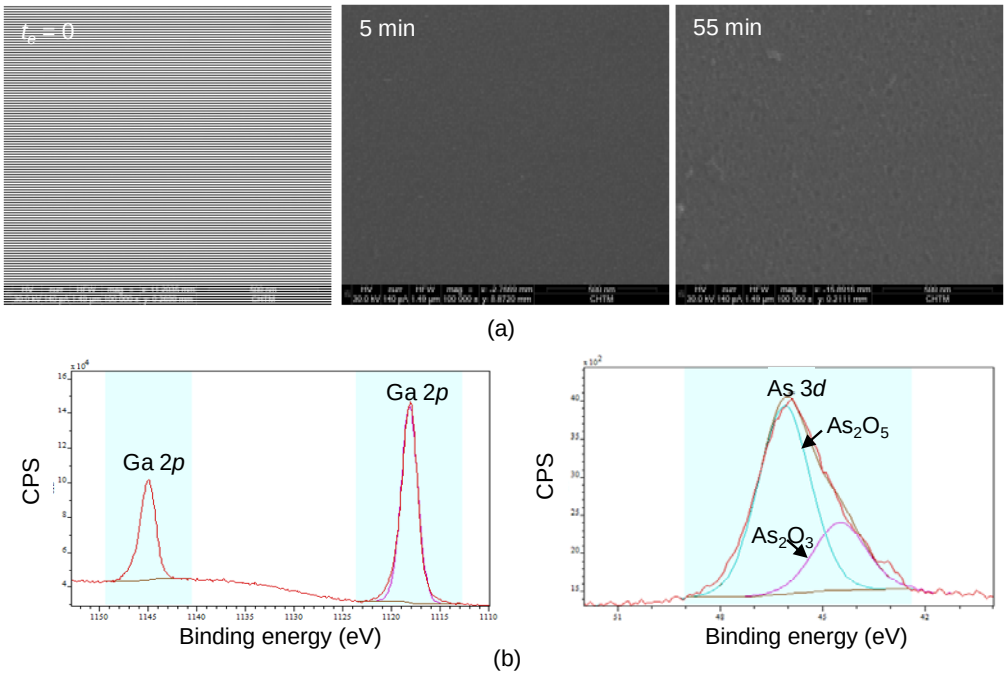


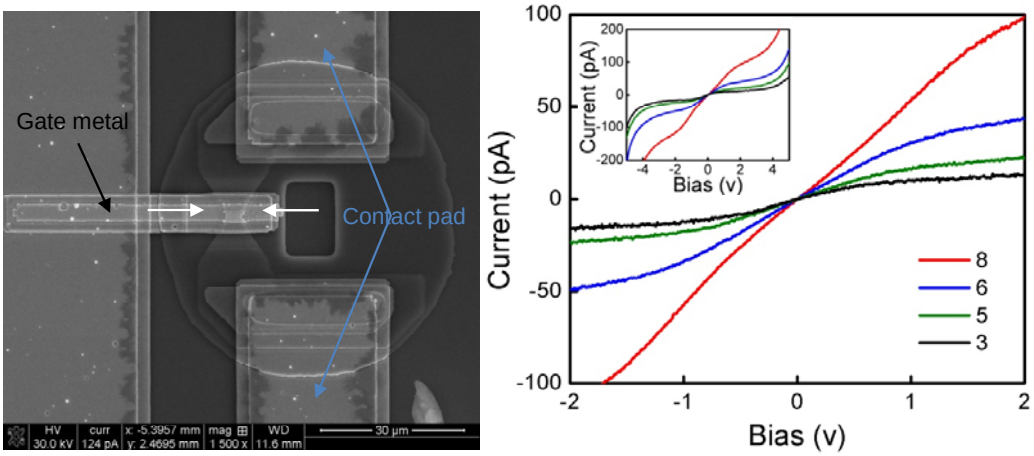
Figure 5 (a) Top-down SEM images of n^+-GaAs surface processed with LPCEO for oxidation time, t_e, = 0 (left), 5 minutes (middle), and 55 minutes (right). (b) XPS spectrum of the n^+-GaAs surface with LPCEO for t_e, = 55 minutes revealing the binding energy of Ga atoms (left) and the status of As atoms (right).

Figure 5(b) is x-ray photoemission spectroscopy (XPS) results of the GaAs oxide prepared by LPCEO. For better accuracy, the oxidation time was set to 55 minutes that provided a oxide layer thick enough for depth profiling. The XPS in Fig. 4 reveals that Ga and As are mostly oxidized to Ga_2O_3 and As_2O_5, As_2O_3 respectively. These basic constituents are similar to the reported data. Also, the ratio of Ga to As is 3.7 - 5.4, implying Ga-dominant oxide by LPCEO. This was expected from the pH ~3.9 set for LPCEO in this work that leads to higher Ga content in an oxide layer. The XPS results therefore confirms that the oxidation of GaAs by LPCEO in this work has been consistently reproduced. However, the ratio of As_2O_5 to As_2O_3 is roughly 2.5, different from the reported data. This could be due to the solubility difference of these chemicals that is related with the long oxidation time for the sample preparation. Further study on the dominance of As_2O_5 is presently under way.

Electrical characterization of sub-100 nm-wide GaAs IPNW arrays

For FET fabrication, gate oxide was implemented with the process based on LPCEO that was developed last year. The thickness of the gate oxide was controlled to ~15 nm by oxidation time. As explained in the last year report and illustrated in Fig. 2(b), each NW channel is fully covered by two different GaAs oxides, the top and sidewalls with ~15 nm-thick GaAs oxide by LPCEO and the bottom with ~20 nm-thick Ga_2O_3 by vertical oxidation of LWO. While the width the NWs in Fig. 3(b) is reduced below sub-100 nm scale, their uniformity along individual

channels has noticeable fluctuation varying 5 - 10 nm. Since the minimum channel width of the array is ~60 nm as seen in Fig. 4(b), the actual channel width after LPCEO is expected to be below 30 nm, slightly less than that illustrated in Fig. 2(b). Then, the cross section of each NW in the array is approximately, ~30 nm in width and ~115 nm in height. This dimension is appropriate to observe fin FET effects. There should be a trade-off between the oxidation time and oxide thickness in the consideration of the uniformity of the oxide layer. Figure 6(a) is an SEM image of the FET with gate metal and contact pads to a source and a drain. In gate metal preparation, off-axis, double deposition of 150-nm Au/10-nm Ti films by 180° rotation with respect to the center of the device was employed for conformal coverage of the channel array with the metal film stack. The arrows in Fig. 6(a) indicate the incident direction of the metal films in electron-beam evaporation. The remaining area of the device was passivated by a SiN_4 film.



(a) (b)

Figure 6 (a) Top-down SEM image of a IPNW FET similar to Fig. 3(b) with gate metal and contact pads. The two white arrows indicate the incident direction of the metal beam in e-beam evaporation. (b) I-V curves from the IPNW FETs with varying *N* from 3 to 8. The inset in (b) reveals the breakdown of the devices at the bias ~ 4V.

Figure 6(b) presents current-voltage (I-V) characteristic of the GaAs IPNW arrays similar to that shown in Fig. 4. The gate was not biased in the I-V curves in Fig. 6(a). The number of NWs in the given arrays, *N*, in Fig. 6 is varied from 3 to 8. All I-V curves confirm ohmic contact but do not show current saturation clearly, unlike the NWs reported last year. The slope of the curves varies at low bias (~ ±0.5V) for $N = 3$ and consistently changes at high voltage (~ ±1.8 V) for $N = 8$. While the current at ±2V plotted in Fig. 6(b) is roughly proportional to *N*, it shows large fluctuations.

In Fig. 6(b), the current at ±2V is ~10 - 100 pA that is extremely low. Last year, we reported a few μA through the ~200 nm × 70 nm channel that was consistent with the current level of the channels in the reported data of which the physical dimension were similar to ours. Such low level current in Fig. 6(b) means high resistance of the NW arrays. Because of the high resistance, the breakdown voltage is reduced below ~5V, as seen in the inset of Fig. 6(b). Moreover, the current leakage to the gate dominates over the current from a source to a drain by this high resistance and seriously degrades the FET performance when the gate is biased.

LPCEO was adapted to implement a gate oxide by direct oxidation of the NW surface to separate the surface states and damage generated in NW preparation from the current flow inside the wire. It was confirmed last year that LPCEO worked at the scale of ~ 200 nm-wide IPNW. This year, we reduced the channel width to ~30 nm and observed serious degradation of device performance by the leakage to the gate. This could be mainly due to the fluctuation of NW width along the channel at such a small scale. Because of width fluctuation and high aspect ratio of the current channel (height/width ~ 130 nm/60nm ~ 2 at the smallest width in the middle of individual channels before LPCEO, ~115 nm/30nm conjectured from the calibration data ~ 4 after LPCEO), the wet oxidation of LPCEO may not proceed into the channel very uniformly, unlike the same oxidation process from a planar surface. In other words, the actual channel cross area of the IPNW after LPCEO could be significantly less than that expected from the calibration results that were performed at a larger scale, for example, because of the stress at the corner edges of the NW. This may explain the extremely small current level in Fig 7(b). Further investigation is presently underway to analyze the LPCEO at sub-100 nm scale 3-dimensional features and to improve the uniformity of NWs.

Epitaxial growth of InAs nanowires on nonplanar Si(001)

One of the solutions for the uniformity control in NW fabrication is epitaxial growth. In this report, growth of InAs NWs as an alternative to GaAs IPNWs that is emerging as a material for III-V FET on Si is investigated. Si(001) which is the main stream in substrate orientation of Si industry is chosen as a substrate.

Epitaxy of InAs on Si suffers from a large lattice mismatch (~7%). To address this difficulty, nanoscale patterned growth (NPG) was adapted and the planar Si(001) substrate surface was processed to an array of nanoscale pillars. Figure 7(a) shows an SEM image of an InAs NW grown on a Si/SiO_2 nanopillar film with MBE. The diameter and height of the pillar are ~100 nm and 250 nm respectively. Its sidewall is passivated by a SiO_2 film. This passivation leads to the selective growth. The contrast difference between Si and SiO_2 reveals the Si core of which the diameter is ~ 32 nm, through the SiO_2 film as denoted with dashed lines in the right of Fig. 7(a). An opening through the SiO_2 passivation for the nucleation of InAs on Si was fabricated at the side of the pillar so that an InAs NW can be initiated from only two (upward and downward) out of eight (111) orientations that are available on the Si pillar. The etching angle of this opening is very important to guide the InAs growth in a single direction and to suppress the other from the two chosen facets in side opening. Unidirectional NWs have a better potential in practical applications. After the fabrication of the opening, the sample was treated by diluted HF to provide a (111) facet for the nucleation in each pillar. At the growth temperature and deposition rate controlled for selective epitaxy of InAs in MBE, an InAs NW was grown on this pillar as shown in Fig. 7(a). The diameter and length of a typical InAs NW at the given growth condition are ~50 - 60 nm and 500 - 600 nm respectively, as denoted in Fig. 7(a). This is very close to the NWs fabricated with top-down process in Fig. 5 in diameter.

The InAs NW on a Si pillar in Fig. 7(a) has a nonplanar surface topography that is not suitable for device processing. Some additional processes are required for actual applications. The primary request is a planar surface for further processing such as metalization for ohmic contact and gate metal. Figures 7(b) and 7(c) show an exemplary process to achieve this planarization. The InAs NW in Fig. 7(a) is conformally covered by a thick SiN_4 film, as shown in Fig. 7(b). It undergoes a planarization etching from the top. Figure 7(c) exhibits an InAs NW of which the lower part is submerged into the SiN_4 film whereas the upper part is protruded from

the SiN_4 film for additional process for metalization. This process is not optimized yet, but evidently provides a top surface more flat than the original surface of Fig. 7(a) and shows a very promising result for future applications. Figure 8 shows the NPG of a 2-dimensional array of such InAs NWs of which the growth is controlled to a single direction with more than 80% yield.

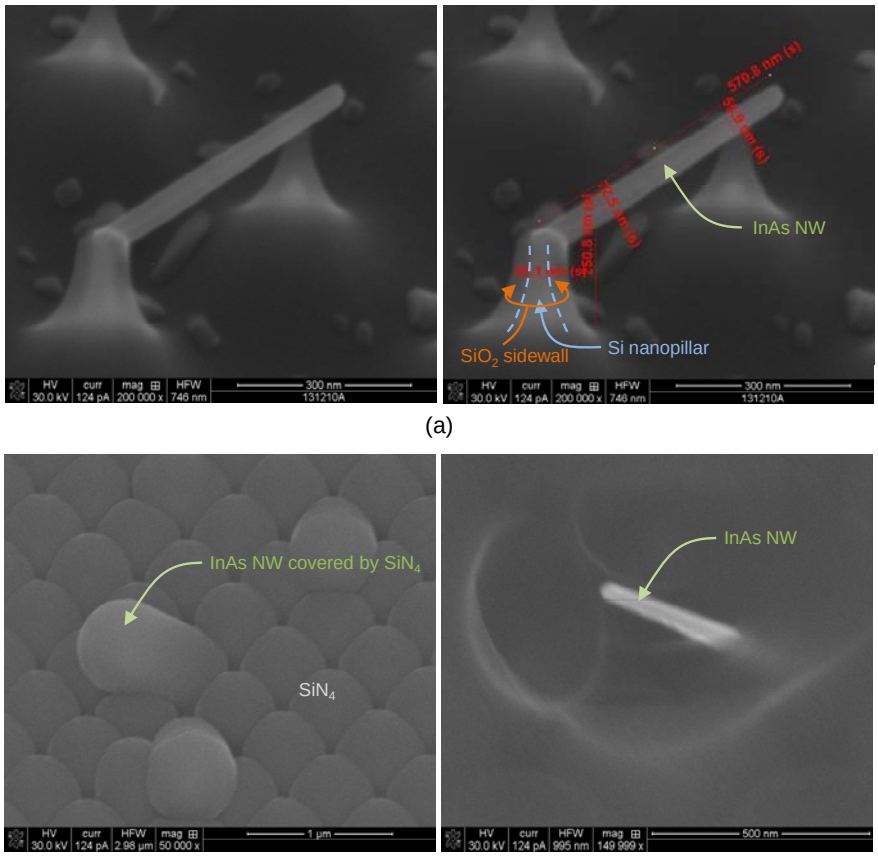
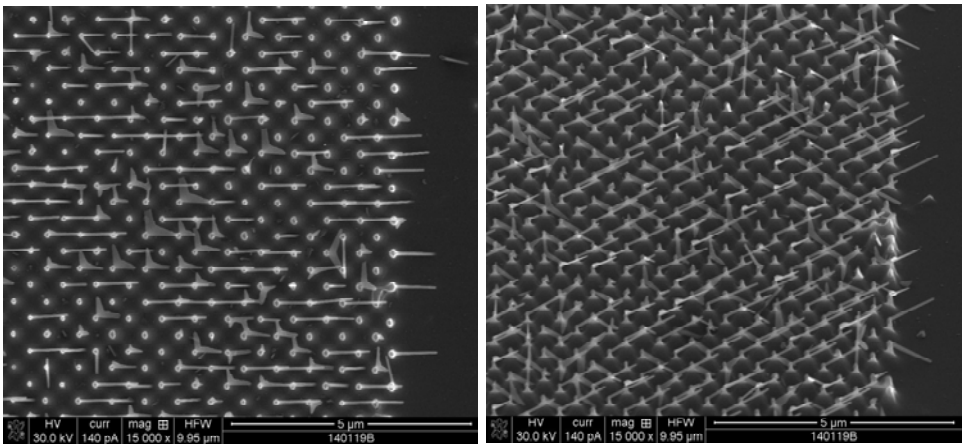


Figure 7 (a) SEM images of an InAs NW grown on a Si nanopillar (left) with dimensions and labels (right). (b) An SEM iamges of InAs NWs conformally covered by SiN_4. (c) An SEM iamge of an InAs NW of which the upper part is exposed above the SiN_4 film by planarization etching. Note the magnification of (b) and (c) different from (a).

Summary and Conclusions

GaAs IPNW MOSFETs with top-down processes have been fabricated and characterized. For this purpose, *i*-line IL and plasma etching were employed. With these techniques, a 500 nm-period 1D array of GaAs IPNWs individually having a 2 μm-long, ~70 nm-wide, 150 nm-high cross area has been achieved. For gate oxide, LPCEO has been adapted to implement ~15 nm-thick GaAs oxide. By sacrificing the NW surface with LPCEO, the channel cross section of an NW is reduced further and the current is conjectured to pass through ~30 nm × 115 nm channel that is sufficient to observe low dimensional transport and fin FET effects. While metalization has been successfully performed on the NW array, further research to improve the uniformity of NWs is required for the investigation of these properties. As an alternative material for better uniformity, epitaxial growth of InAs NW on a Si nanopillar has been examined.



(a) (b)

Figure 8 SEM images of an InAs NW array grown on a 420 nm-period, 2D Si nanopillar pattern in (a) top-down and (b) 45°-tilted side view. Each NW in (b) corresponds to the InAs NW in Fig. 7(a).

What opportunities for training and professional development has the project provided?
If the research is not intended to provide training and professional development opportunities or there is nothing significant to report during this reporting period, state "Nothing to Report." Describe opportunities for training and professional development provided to anyone who worked on the project or anyone who was involved in the activities supported by the project. "Training" activities are those in which individuals with advanced professional skills and experience assist others in attaining greater proficiency. Training activities may include, for example, courses or one-on-one work with a mentor. "Professional development" activities result in increased knowledge or skill in one's area of expertise and may include workshops, conferences, seminars, study groups, and individual study. Include participation in conferences,workshops, and seminars not listed under major activities.

A manuscript has been prepared for publication. It is included as Appendix A.

How have the results been disseminated to communities of interest?
If there is nothing significant to report during this reporting period, state "Nothing to Report." Describe how the results have been disseminated to communities of interest. Include any outreach activities that have been undertaken to reach members of communities who are not usually aware of these research activities, for the purpose of enhancing public understanding and increasing interest in learning and careers in science, technology, and the humanities.

Two patent disclosures were filed with the UNM patent office during the course of this work.

A. Method of making heteroepitaxial structures and device formed by the method. (Disclosed July 14, 2011)

Inventors: Steven R. J. Brueck, Stephen D. Hersee and Seung Chang Lee

A method has been developed to optimally grow GaN and its alloy system with AlGaN on a Si(100) surface, configured for leading-edge electronics. The method utilizes current lithographic capabilities as well as industry standard Si and is thus scalable. Another advantage of cubic GaN is the absence of a built-in polarization field that allows normally-off operation – important for low power consumption circuits.

B. Gate-all-around metal-oxide-semiconductor transistors with gate oxides. (Disclosed Dec. 13, 2012)

Inventors: Steven R. J. Brueck, Seung-Chang Lee and Daniel Feezell)

A method and structure for a semiconductor transistor, including various embodiments. In embodiments, a transistor channel can be formed between a semiconductor source and a semiconductor drain, wherein a transistor gate oxide completely surrounds a transistor channel and a transistor gate metal completely surrounds the transistor gate oxide. Related fabrication processes are presented for similar device embodiments based on a Group III-V semiconductor material and silicon-on-insulator materials.

What do you plan to do during the next reporting period to accomplish the goals?
If there are no changes to the agency-approved application or plan for this effort, state "No Change." Describe briefly what you plan to do during the next reporting period to accomplish the goalsand objectives.

This is a final report. There are no further activities planned.

Appendix A: Manuscript prepared for submission to archival journal

Top-down, in-plane nanowire GaAs MOSFET by focused ion beam milling and chemical oxidation

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Abstract

The top-down fabrication of an in-plane nanowire (NW) GaAs metal-oxide-semiconductor field-effect transistor (MOSFET) by focused-ion beam (FIB) etching and chemical oxidation is reported. The device has a semiconductor-on-insulator structure with an n^+-GaAs/Al_2O_3 layer stack implemented by lateral hydrolyzation oxidation. A 2 μm-long channel having an effective cross section ~70 nm × 220 nm is directly fabricated into the n^+-GaAs layer by FIB etching. The channel is electronically isolated from the substrate by the Al_2O_3 layer and is effectively an in-plane NW epitaxially connected to the source and drain for a planar MOSFET within a single layer. The NW channel is surrounded by an ~15 nm-thick gate oxide produced by liquid-phase chemically enhanced oxidation. The device has threshold voltage ~0.14 V and peak transconductance ~24 μS (109 μS/μm) with a subthreshold swing ~ 110-150 mV/decade and a on/off ratio of drain current ~ 10^3.

I. Introduction

Recently, III-V semiconductor *in-plane* nanowire (NW) field-effect transistors (FETs) have been reported by several research groups [1]-[4]. Most of them are based on GaAs. For smaller GaAs NWs, bottom up fabrication relying on vapor-liquid-solid (VLS) growth mechanism is preferentially used rather than top-down processing [1], [2], [4]. For integration with Si microelectronics for their high electron mobility, however, top-down fabrication of in-plane NWs is particularly attractive since the deterministic placement, size uniformity, and orientation-independent processing is directly related to high yield and compatibility with large-scale circuits. In contrast to VLS approaches, the top-down fabrication is catalyst-free and employs high purity, well developed III-V epitaxy technologies. Furthermore, metal-oxide-semiconductor (MOS) FETs have a larger voltage swing, more adaptable to digital integrated circuits, than metal-semiconductor (MES) FETs where the low Schottky barrier restricts the operation to relatively low gate biases [5]. In this work, top-down fabrication of an in-plane NW GaAs MOSFET by focused ion beam (FIB) milling is demonstrated with the gate oxide fabricated by liquid phase chemical-enhanced oxidation (LPCEO) [6].

FIB is an easily accessible nanoscale processing technique that uses maskless direct etching without any separate lithography steps; however, FIB leaves damage on etched sidewalls such as amorphorization and ion-implantation that has to be removed during subsequent processing. Lacking the high quality Si-SiO_2 interface, the III-V gate-oxide material is an inherent issue. LPCEO, a low-temperature chemical oxidation process for III-V semiconductors is used both to relieve the damage from FIB by transforming the etched sidewalls to a gate oxide film and further decrease the channel cross section by consuming the channel material in the oxidation.

Our device is on top of an Al_2O_3 layer that is transformed, post-growth, from $Al_{0.98}Ga_{0.02}As$ underneath the device by lateral hydrolyzation oxidation (LHO) forming a semiconductor on insulator (SOI) structure [7]. LHO has been widely examined over III-V semiconductors [8]-[10]. Several articles have reported MESFETs and MOSFETs on SOI prepared by LHO [11]-[14]. The SOI in this work allows the use of micro-scale ohmic source/drain pads directly connected to the NWs forming planar devices in a single epitaxial layer. The nm-scale channel fabricated by FIB is then effectively an in-plane NW with suppression of the current leakage to the substrate by the insulator layer. The effective channel cross section and length of the GaAs NW in the present device is approximately 70×220 nm^2 and 2 μm. In LHO, however, unexpected vertical oxidation into the doped GaAs layer that forms a heterostructure with the $Al_{0.98}Ga_{0.02}As$ layer is observed. This could be critical to top-down process using SOI from LHO in the control of the height and surface roughness of the current channel. While there are many literature reports of LPCEO for the application to gate oxide, it has not been examined for nanoscale devices [6]. Material as well as electrical characteristics of a nm-scale gate oxide prepared by LPCEO need to be analyzed. This work investigates the material characteristics related with LHO and LPCEO at the nanoscale. The importance of the vertical oxidation is addressed. Also, the top-down fabrication of in-plane NW GaAs MOSFETs by FIB milling and their characteristics associated with the NW channel surrounded by ~15 nm-thick gate oxide from LPCEO are reported.

II. Device Fabrication

Figure 1(a) shows the layer structure used in this work grown on a semi-insulating GaAs(001) substrate by molecular beam epitaxy (MBE). It consists of a 100 nm-thick, Si-doped n^+-GaAs (doping concentration > 2×10^{18} cm^{-3}) and a 500-nm thick $Al_xGa_{1-x}As$ (x~0.98) layer

atop an undoped GaAs buffer. The top layer will be used for the device fabricated with a top-down process and the bottom $Al_xGa_{1-x}As$ (x~0.98) layer will be converted to Al_yO_3 (y~2). The process flow of device fabrication is schematically illustrated in Fig. 2. The device process includes three major steps: LHO to form the local SOI structure in Fig. 2(a); FIB milling to fabricate an in-plane NW in Fig. 2(c); and LPCEO to remove and transform the FIB-damaged layer into a gate oxide surrounding the NW in Fig. 2(d). Additional metallization steps complete the transistor fabrication.

A. LHO

The first major step is the transformation of the $Al_{0.98}Ga_{0.02}As$ layer underneath the conducting GaAs layer to Al_2O_3 by LHO. A hot water vapor-filled furnace at ~460°C was employed for this process. To avoid any oxidation from the top during LHO, the surface was protected by a ~100 nm-thick SiO_2 film deposited by electron-beam evaporation. A trench penetrating through the $Al_{0.98}Ga_{0.02}As$ layer indicated in Fig. 2(a) was prepared adjacent to the device site to localize LHO to the immediate device vicinity by controlling the access of water vapor. This minimizes the stress due to the volume contraction (~10% in thickness reduction) of the $Al_{0.98}Ga_{0.02}As$ layer by LHO [15]. Figure 3 presents a plot of oxidation rate of $Al_{0.98}Ga_{0.02}As$, r_{AlGaAs}, vs oxidation time measured with the layer structure in Fig. 1(a). As shown in Fig. 3, the oxidation rate decelerates with time as expected since it relies on the diffusion of water vapor through the oxidized region that increases with time and slows the reaction. This agrees well with the reported data [7],[10].

In cross sectional view, it is observed that LHO induces not only lateral oxidation of $Al_{0.98}Ga_{0.02}As$ but also vertical oxidation into the upper n^+-GaAs layer during oxidation process in a furnace. A scanning electron microscopy (STEM) image in Figure 4(a) reveals the vertical

oxidation that simultaneously proceeds into the top and bottom epitaxial GaAs layers from GaAs/$Al_{0.98}Ga_{0.02}As$ (or GaAs/Al_2O_x) interface along with LHO that was prepared for this purpose. In our experiment, this vertical oxidation into GaAs is critically affected by Si doping. From Fig. 4(a), the vertical oxidation rate, $r_{GaAs,\perp}$, was measured as ~4 nm/min for ~2×10^{18} cm^{-3} (the upper interface) and ~1 nm/min for ~1×10^{17} cm^{-3} (the lower interface) respectively at the present oxidation conditions, very different from r_{AlGaAs} which is on a μm/min scale. Generally, $r_{GaAs,\perp}$ is negligible for undoped GaAs [7],[16]. These results suggest that $r_{GaAs,\perp}$ is enhanced with Si doping concentration. Such Si dopant-dependent LHO has not been reported previously. It may be related to Al diffusion into the GaAs layers across the heterointerface activated by Si atoms which cause Al intermixing at doped AlGaAs/GaAs heterointerfaces in annealing [17]. It is known that Al diffusion is proportional to Si doping concentration with a fourth power dependence. Figure 4(b) shows a magnified transmission electron microscopy (TEM) image of region A indicated in Fig. 4(a). The interface between GaAs and Ga_2O_3 has some fluctuation in flatness. A high resolution TEM image in Fig. 4(c) reveals the interface fluctuation including a transition zone between them (i.e., a mixed region) is extended up to ~5 nm at the given LHO conditions.

The vertical oxidation is very slow compared with lateral oxidation into AlGaAs but could be critical for the device targeted in this work since the thickness of the GaAs conducting layer is only ~100 nm and it can be fully oxidized in ~25-minute LHO, eliminating the current channel. The device of this work includes μm-scale areas in the n^+-GaAs layer for source/drain pads which are connected to the NW in a single epitaxial layer. The finite $r_{GaAs,\perp}$ of ~ 4 nm/min limits the oxidation time for the given 100 nm-thick n^+-GaAs layer atop AlGaAs layer. To retain ~85 nm-thick GaAs for an NW channel before LPCEO which will also consume this layer for

gate oxide, the oxidation time shouldn't exceed ~5 minutes and the corresponding d_{ox} becomes ~ 16 to 18 μm from Fig. 3. Larger pad areas can achieve better ohmic contact. Based on this estimate, the largest width of the pad area was set to 14 μm so that the entire device could be implemented on the SOI structure. Assuming the transition zone width between GaAs and Ga_2O_3 is proportional to oxidation time, ~ 1 nm-wide fluctuations at the interface is expected.

The vertical oxidation leaves Ga_2O_3 as a main product by substituting As atoms with oxygen atoms, like AlGaAs [7]. It also incurs a volume shrinkage, like Al_2O_3. Beside the cumulative stress at GaAs/Al_2O_3 interface due to the volume contraction in LHO, therefore the vertical oxidation is another limitation on LHO in top-down SOI GaAs MOSFETs if heavily-doped GaAs is employed for a device.

The resulting SOI structure suppresses the current leakage through the substrate. After LHO, the layer structure underwent a standard FET process to define a device. The n^+-GaAs conducting layer in SOI was processed into a 14 μm-wide, 180 μm-long stripe with photolithography and chlorine-based plasma etching, as illustrated in Figs. 1(b) and 2(b). The long side is parallel to the LHO trench so that the stripe is located atop the ~17-μm wide Al_2O_3 film. Two 10 × 60 μm^2 ohmic metals were deposited at both ends for source and drain contacts as indicated in Fig. 1(b). As a result of the SOI structure, there is no source-to-drain leakage current through the Al_2O_3 layer within the measurement limit of 10^{-10} A when the channel between source and drain was removed.

B. FIB milling

As shown in Fig. 2(c), a 200 nm-thick Si_3N_4 film passivated the device structure during the FIB channel fabrication. Figure 5 presents the ion-beam images of the stripe before and after FIB etching. As seen in Fig. 5(a), a 4 μm-wide opening was fabricated into the Si_3N_4 film across the channel area (perpendicular to the trench) at the middle of the stripe by CF_4 plasma etching. The channel in this opening area was narrowed by FIB etching. As shown in Fig. 5(b) and its inset, two rectangular regions in the opening were directly etched out to leave a 250 nm-wide, 2 μm-long channel. The etch depth was controlled to touch down to the Al_2O_3 layer. The channel in Fig. 5(b) behaves like an in-plane NW shown in Fig. 1(b) that is electronically isolated from the substrate by SOI and directly connected to ohmic pads in a single epitaxial layer. To keep from damaging the channel from any during the FIB process, the top surface was passivated with a Ti/photoresist (PR) film stack during milling. After FIB etching, the Ti film was simply removed with a lift-off process.

C. LPCEO

The last major step in the NW MOSFET fabrication was formation of the gate oxide surrounding the in-plane NW channel by LPCEO. As mentioned earlier, this contributes to the relief of the damage on the sidewalls in FIB milling through transformation into an oxide consuming the damaged areas with LPCEO. Since a ~15 nm-thick Ga_2O_3 film is already embedded between the NW channel and the Al_2O_3 film as a byproduct of LHO, the pH of the etchant was set to ~3.9 to increase the Ga/As ratio in the oxide film so that the in-plane NW is surrounded by similar materials [18]. LPCEO was performed at 70°C and it proceeded only at the opening in the Si_3N_4 film shown in Figs. 2(d) and 5(a).

The roughness of the oxidation front (boundary between oxidized and unoxidized GaAs) in LPCEO is also important for the current passing through a NW channel with an LPCEO gate oxide because it is related to the surface scattering of electrons. The roughness of the interface has been investigated with on a GaAs substrate [18]. Particularly, it is reported that a spiky oxidation proceeding with undercut at the boundary of a PR film defining an etched area is critical. To avoid this issue that could be crucial at the nm-scale, the etching boundary [identical to the Si_3N_4 boundary in Fig. 5(a) self-aligned for LPCEO] was designed to locate ~ 1 μm away from the NW in both sides and this issue does not seriously affect the device performance. In this work, the surface morphology of the oxide layer was examined with the variation of oxidation time or oxide thickness for the relation of surface morphology to oxide thickness (time). Figure 6(a) is top-down view SEM images from planar n^+-GaAs without LPCEO on the left, with 9 minute LPCEO in the middle, and 55 minute LPCEO on the right. A 9 minute LPCEO corresponds to about 15 nm-thick oxide as discussed later and 55 min oxidation results in ~100 nm-thick oxide on the channel. The surface morphology is degraded as the oxidation time increases. Degradation of surface morphology is evident for 55 min but is not noticeable up to 9 minute etching at the given magnification. This means LPCEO may not be adequate for very thick oxide but is acceptable for thin oxide of this work in surface morphology.

Figure 6(b) shows x-ray photoemission spectroscopy (XPS) results of the GaAs oxide prepared by LPCEO. For better accuracy, the 55 minute-oxidized sample of Fig. 6(a) was employed in this analysis since it provided an oxide layer thick enough for depth profiling. The XPS in Fig. 6(b) reveals that Ga and As are mostly oxidized to Ga_2O_3 and As_2O_5, As_2O_3 respectively. These basic constituents are similar to the reported data.[18] Also, the ratio of Ga to As is 3.7 - 5.4, implying Ga-dominant oxide by LPCEO. This was expected from the pH ~3.9 set

for LPCEO in this work that leads to higher Ga content in an oxide layer. The XPS results therefore confirm that the oxidation of GaAs by LPCEO in this work has been consistently reproduced. However, the ratio of As_2O_5 to As_2O_3 is roughly 2.5, different from the reported data [18]. This could be due to the solubility difference of these chemicals that is related with the long oxidation time for the sample preparation. A study on the dominance of As_2O_5 is presently under way.

Oxidation speed by LPCEO was calibrated with using the conductance of the GaAs channels. For calibration, three additional 20-μm long, 600-nm wide, 500-nm thick n^+-GaAs channels which have the thickness of 5 × that of the NW channel for better accuracy were fabricated on semi-insulating GaAs and the change of their current was measured by taking the ratio of channel current before and after LPCEO ($I_{d,a}/I_{d,b}$, where *a* and *b* refer to after and before LPCEO) with etching time, t_e, varied up to 90 minutes. Before LPCEO, the channels were processed with diluted NH_4OH for the removal of any native oxide.

Figure 7 (left axis) presents a plot of $I_{d,a}/I_{d,b}$ versus t_e. As expected, normalized current decreases from 1 to 0.37 with a slight deceleration of the oxidation speed as t_e increases to 90 minutes. In Fig. 3(b) (right axis), oxidation depth (or oxide film thickness) estimated from $I_{d,a}/I_{d,b}$ is shown under the assumption of uniform oxidation from all three sides inward to the channels resulting in a rectangular cross section, as illustrated in the inset of Fig. 7. The oxidation into the semi-insulating substrate was not considered. In Fig 7. $I_{d,a}/I_{d,b}$ has a nonlinear dependence on t_e but the oxidation depth is almost proportional to the current ratio, as expected. The LPCEO oxidation rate, r_L, is ~ 1.7-1.9 nm/min, that is low enough to assume a linear dependence in the range of t_e examined in this work. This is even lower than $r_{GaAs,\perp}$ for n^+-GaAs in LHO and suitable for gate oxide formation where nm-scale thickness control is required. Based on this

result, the oxidation time was adjusted to proceed into the channel for ~15 nm from the surface (~9 minutes); similar to the thickness of the Ga_2O_3 at the bottom. Thus, the effective cross section of the conducting channel for NW MOSFET is reduced to ~70 nm × 220 nm; the active length is 2 μm; and the thickness of the gate oxide film surrounding the channel is ~15 nm, as illustrated in Fig. 2(e). Conventional Au/Ni/Au/Ge and Au/Ti film stacks were used as ohmic and gate metals.

III. Device characteristics

This junctionless NW MOSFET is very different from typical FETs. Figure 8(a) and its inset show I-V curves between source and drain of the n^+-GaAs conducting stripe in SOI before and after FIB milling and LPCEO without any gate bias. The current after LPCEO is ohmic with a saturation region but is only about 20 - 30% of the current before the oxidation. This is noticeably smaller than that expected from geometric considerations based on the NW cross section illustrated in Fig. 2(e) and the inset of Fig. 7. This inconsistency could be due to the different physical dimensions; the smaller NW may have more anisotropic oxidation profile resulting from its shape and the stress associated with layer structure than the larger ones used for calibration. Another possibility is any residual defects play a larger role as the channel width decreases. Moreover, defect-related fixed charges in the oxide could reduce the active cross section as suggested by the source-drain current results. Thus, ~15 nm can be regarded as the thinnest gate oxide thickness from LPCEO available at the given NW channel. The NW width after FIB, 250 nm, is ~1.8% of the original channel width, 14 μm. The current of the stripe through the NW channel is ~1% of that before FIB etching implying that the effective channel cross section is somewhat smaller than the physical dimensions as a result of damage and surface pinning, but conclusively showing that the channel is not fully depleted as a result of the FIB

process. The NW channel resistance dominates the current in the stripe implying that any source-gate and drain-gate resistances do not impact the device performance.

Figure 8(b) shows the I-V curve of the in-plane NW MOSFET for gate bias, V_g, from -0.2 to 1.0 V with a 0.2 V step. A linear region is clearly defined together with a saturation region. This implies an ohmic contact to the stripe and as a result to the NW. Because the ohmic source/drain pads are removed from both ends of the NW by a distance more than 5 × NW length, the enhancement of the drain current, I_d, at high drain bias, V_d, due to the channel shortening from the depletion region of the drain that is typically observed in conventional FETs is not expected in the saturation region. Instead, I_d in saturation region slightly decreases with increasing V_d for the range of bias examined in this work. This becomes clearer at larger V_g. As mentioned earlier, there will be a some roughness along the GaAs/oxide interface generated from both LHO at the bottom and LPCEO at the side walls. This could result in electron scattering by the GaAs/oxide interface along the NW that becomes more significant among the carriers highly confined in the NW channel at larger bias. In the inset of Fig. 8(a) [Fig. 8(b)], I_d at $V_g = 0$ is only about ~0.5 μA (0.15 μA) at saturation region without (with) gate metal even though the NW is heavily doped by Si. While an NW MOSFET can exhibit both enhancement and depletion modes at the present doping level, this implies that the NW channel surrounded by the oxide films is not completely depleted by the GaAs/oxide interface states and works in enhancement rather than depletion mode.

Figure 8(c) is a plot of I_d versus V_{gs} revealing the transconductance characteristic of the device. The threshold voltage. V_T, is ~0.14 V. The I_{on}/I_{off} ratio is ~10^3 and the subthreshold swing is conservatively measured as ~110 - 150 mV/dec (see inset). The peak g_m is ~ 24 μS at $V_d = 0.9$ V (~109 μS/μm). These values are comparable to those reported with GaAs NW MESFETs

fabricated by bottom-up process except for the positive V_T that is feasible in MOSFET structures [1]-[4]. This implies that the the roughness on the GaAs/oxide interfaces examined in this work is does not impact device performance too negatively. Table I shows the performance summary of the GaAs NW FETs recently reported, including the device of this work. Figure 8(d) is a plot of leakage current to gate vs *Vg*. The result is a conventional MOSFET characteristic for low *Vg* [1]that exhibits a leakage current level at forward bias roughly by an order of magnitude improved over that for a VLS-grown FET. The LPCEO gate oxide therefore can be another strong candidate of gate oxide of III-V NW MOSFET.

A couple of issues related to the fabrication which are not fully understood should be addressed in future work. One is the extent of the relief of the NW sidewall surface damage by Ga ions during FIB etching by LPCEO. The other is the material properties of the LPCEO oxide used for gate oxide of the NW MOSFET such as stoichiometry and thickness. Also, the thickness uniformity along the NW that is critical in surface or interface scattering of the carriers along the NW requires in-depth study to understand I_d-V_d relation at high bias.

IV. Summary and conclusions

The top-down fabrication of a SOI in-plane NW GaAs MOSFET by FIB etching has been demonstrated. For the gate oxide, a ~15 nm-thick LPCEO oxide was employed. FIB fabricates in-plane NWs by direct etching and reaches ~200 nm channel width with a maskless, single-step lithography process. With a 2 μm long, ~70 nm × 220 nm effective cross section NW channel, the device exhibits V_T ~0.14 V and peak g_m ~24 μS with a subthreshold slope of ~110-150 mV/dec, similar to the characteristics observed in bottom-up, VLS-grown NW GaAs MESFETs. Therefore, top-down NW process by FIB is proven as a promising fabrication technology for

nanoscale electronic devices together with LPCEO that can provide a gate oxide applicable to NW scale devices.

Table I Summary of the in-plane NW GaAs FETs recently reported.

Ref.	Growth/ Fabri-cation	Channel Cross Section	Structure	Substrate	Gate/ Barrier	g (μS/μm)	SS (mV /dec)	I_{on}/I_{off}
[1]	VLS	diameter~ 250 nm	MESFET	SI GaAs	Ti/Au Schottky	23	150	240
[2]	VLS	<250 nm	HEMT	SI GaAs	AlGaAs	83	181	~10^4
[3]	Aniso-tropic etching/ Pick and place	~200 nm	MESFET	Plastic	Ti/Au Schottky	17	<150	<10^7
[4]	VLS	~250 nm	MESFET	(110) SI GaAs	Ti/Au Schottky	76	169	850
This work	MBE/FIB	Rectangular 70 nm× 220 nm	MOSFET	Al_2O_3	Trigate /Ga_2O_3 LPCEO	109	110-150	~10^3

References

[1] S. A. Fortuna and X. Li, "GaAs MESFET with a high mobility self-assembled nanowire channel," *IEEE Elec. Dev. Lett*., **30**, 593-595 (2009).

[2] X. Miao and X. Li, "Scalable monolithically grown AlGaAs-GaAs planar nanowire high-electronc-mobility transistor," *IEEE Elec. Dev. Lett*. **32**, 1227-1229 (2011).

[3] C. Yoon, G. Cho, and S. Kim, "Electrical characteristics of GaAs nanowire-based MESFETs on flexible plastics," *IEEE Trans. Elec. Dev*., **58**, 1096 (2011).

[4] R. Dowdy, D. A. Walko, S. A. Fortuna, and Xiuling Li, "Realization of unidirectional planar GaAs nanowires on GaAs (11) substrates," *IEEE Elec. Device Lett*., **33**, 522-524 (2012).

[5] M. Shur, *GaAs Devices and Circuits*, p448, Plenum Press (New York, 1987).

[6] *For review*, R. Korbutowicz and J. Prazmowska , *Wet Thermal Oxidation of GaAs and GaN Semiconductor Technologies*, J. Grym (Ed.), ISBN: 978-953-307-080-3, InTech (2010).

[7] J. M. Dailesasse, N. Holonyak, Jr., A. R. Sugg, T. A. Richard, and N. EI-Zein, "Hydrolization oxidation of $Al_xGa_{1-x}As$-AlAs-GaAs quantum well heterostructures and superlattices," *Appl. Phys. Lett*., **57**, 2844-2846 (1990).

[8] F . A . Kish , S. J. I. Caracci , N. Holonyak, Jr., J. M. Dallesasse, A. F. L. Sugg, R. M. Fletcher, C. P. Kuo, T. D. Osentowski, and M. G, Craford, " Native-oxide stripe-geometry $In_{0.5}(AI,Ga_{1-x})_{0.5}P$-$ln_{0.5}Ga_{0.5}P$ heterostructure laser diodes," *Appl. Phys. Lett*., vol. **59**, no. 3, pp. 354-356, July, 1991.

[9] O. Blum, K. M. Geib, M. J. Hafich, J. F. Klem, and C. I. H. Ashby, "Wet thermal oxidation of AlAsSb lattice matched to InP for optoelectronic applications," *Appl. Phys. Lett.*, vol. **68**, no. 22, pp. 3129-3131, May, 1996.

[10] *For review*, J. M. Dallesassea and N. Holonyak, Jr., " Oxidation of Al-bearing III-V materials: A review of key progress," *J. Appl. Phys*., vol. **113**, 051101, 2013, and references therein.

[11] E. I. Chen, N. Holonyak, Jr., and S. A. Maranowski, "$Al_xGa_{1-x}As$-GaAs metal-oxide semiconductor field effect transistors formed by lateral water vapor oxidation of AlAs," *Appl. Phys. Lett*., vol. **66**, no. 20, pp. 2688-2690, May, 1995.

[12] P. Parikh, P. Chavarka, and U. K. Mishra, "GaAs MESFETs on a truly insulating buffer layer: Demonstration of the GaAs on insulator technology," *IEEE Elec. Device Lett.*, vol. **18**, no. 3, pp. 111–114, Mar. 1997.

[13] C. Zheng, R. Coffie, D. Buttari, J. Champlain, and U. K. Mishra, " Oxidation Control of GaAs pHEMTs for High Efficiency Applications," *IEEE Elec. Device Lett*., vol. **23**, no. 7, pp. 380-382, July, 2002.

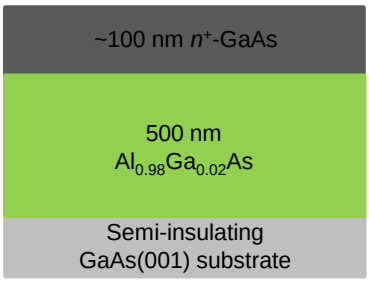
[14] S. Y. Tzeng, M. J. Cich, R. Zhao, H. Feick, and E. R. Weber, "Generation-recombination low-frequency noise signatures in GaAs metal–semiconductor field-effect transistors on laterally oxidized AlAs," *Appl. Phys. Lett.*, vol. **82**, no. 7, pp. 1063-1065, Feb. 2003.

[15] H.-H. Wang, D. W. Chou, J.-Y. Wu, Y.-H. Wang, and M.-P. Houng, "Surface oxidation kinetics of GaAs oxide growth by liquid phase chemical-enhanced technique," *J. Jpn. Appl. Phys*., Part 1, vol.**39**, no. 7B, 4477-4480, July, 2000.

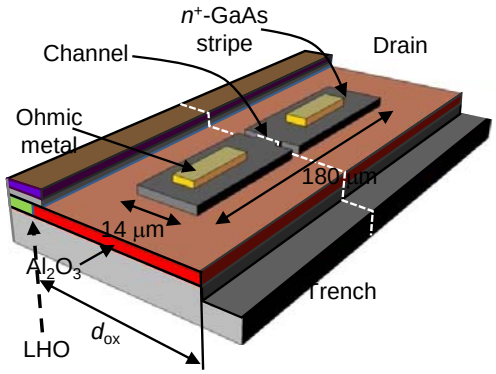
[16] O. Durand, F. Wyckzisk, J. Olivier, M. Magis, P. Galtier, A. De Rossi, M. Calligaro, V. Ortiz, V. Berger, G. Leo and G. Assanto, "Contraction of aluminum oxide thin layers in optical heterostructures," *Appl. Phys. Lett*. **83**, 2554-2556 (2003).

[17] R. Y. Li,_Z. G. Wang, B. Xu, P. Jin, X. Guo, M. Chen, 'Interface of wet oxidized AlGaAs/GaAs distributed Bragg reflectors," *Appl. Phys*. *A*, vol. **86**, pp. 19–22, 2007.

[18] D. Sun and P. Mei, in *Semiconductor quantum wells intermixing*, ed. E. H. Lee, Ch. 7, pp. 287, Gordon and Breach Science Publisher (Amsterdam, 2000).



(a)



(b)

Figure 1 (a) A schematic cross section of the layer structure grown by MBE. (b) a 14 × 180 μm stripe device in SOI after FIB and LHO where the 500 nm-thick $Al_{0.98}Ga_{0.02}As$ layer was reduced to ~440 nm thick Al_2O_3 film because of volume shrinkage. The white dashed line across the structure corresponds to the cross sections in Fig. 2.

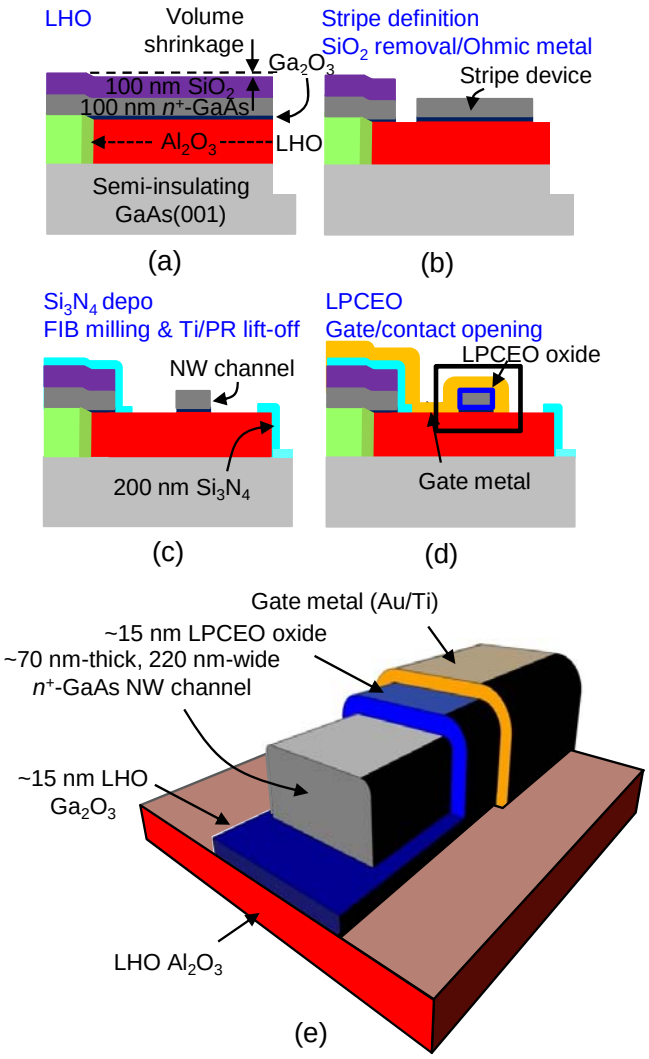


Figure 2 (a) to (d) A schematic illustration of process flow in cross sectional view along the white line in Fig. 1(b). (e) A magnification of the black rectangle in (d) with cutaway portions.

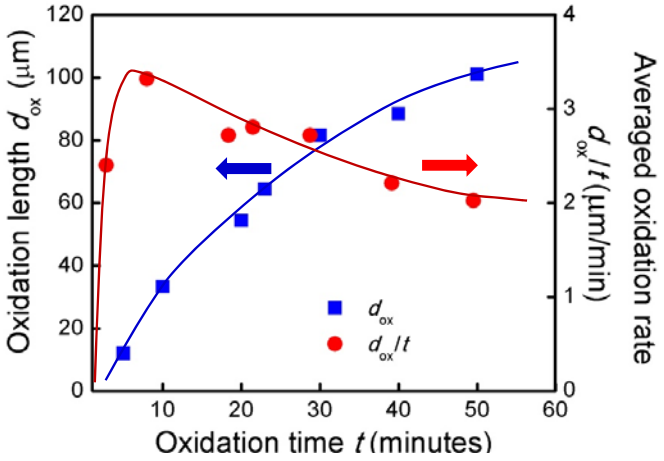


Figure 3 A plot of oxidation length (left *y*-axis) and average oxidation rate (right *y*-axis) vs oxidation time. The lines are for eye-guiding.

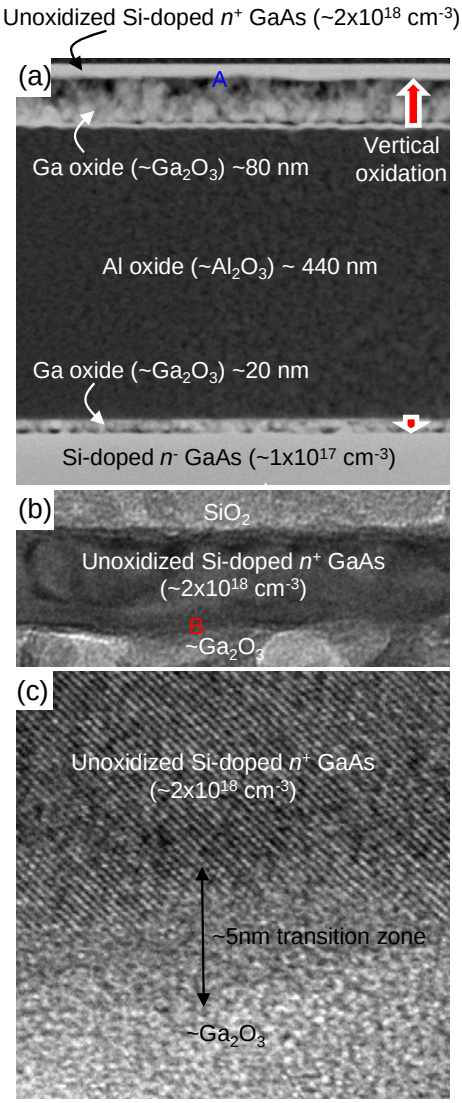


Figure 4 (a) A cross sectional STEM image of the sample after LHO. Vertical oxidation is indicated with red bold arrows. It should be noted that the layer structure employed in this figure is different from that in Fig. 1(a). (b) A TEM magnification of region A in (a). (c) A high resolution TEM of region B in (b).

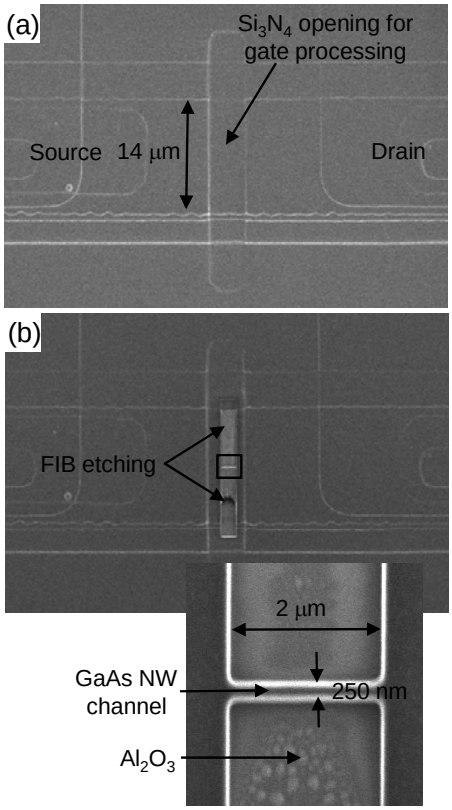
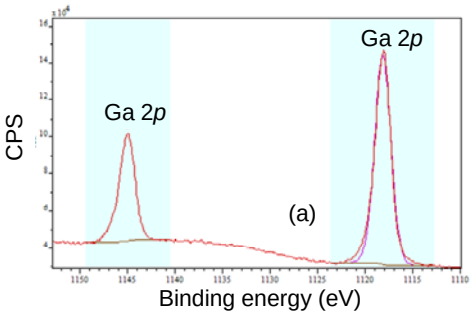
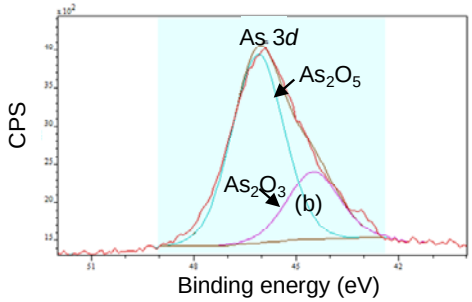


Figure 5 Ion-beam images of a top-down, 250nm-wide, SOI GaAs NW (a) before and (b) after FIB milling with the inset for the magnification of a rectangle in (b). The surface is passivated with Ti/photoresist film stack.

(a)





(b)

Figure 6 (a) Top-down view SEM images from planar n^+-GaAs without LPCEO (left), with 9 minute LPCEO (middle), and 55 minute LPCEO (right). (b) XPS spectra of the GaAs oxide prepared by LPCEO at the right in (a)

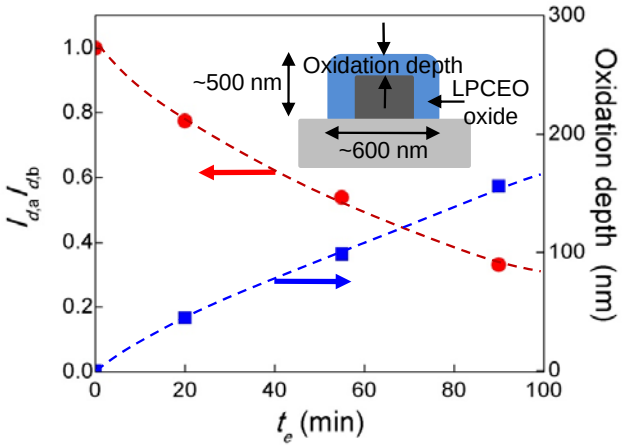
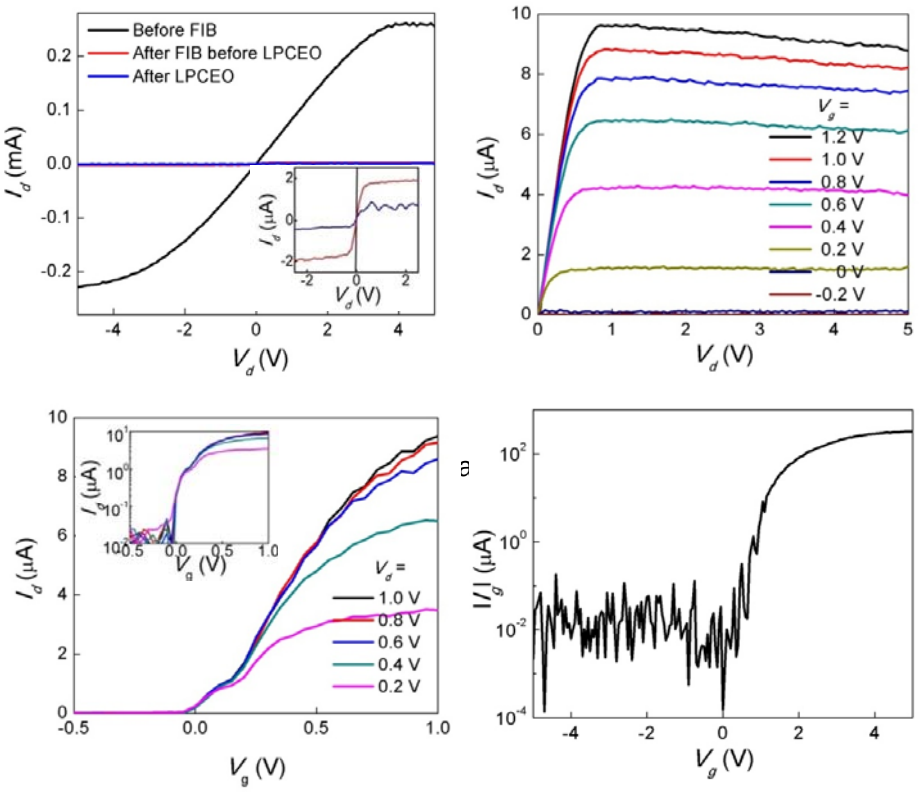


Figure 7 A plot of current ratio (after/before LPCEO, left *y*-axis) and corresponding oxidation depth (right *y*-axis) versus oxidation time measured with 600-nm wide, 500 nm-thick GaAs channels. The inset is a schematic illustration of the cross section. The dashed lines are for guiding eyes.



(b)

Figure 8 (a) I_d-V_d curves before FIB (black), after FIB (red), and after LPCEO (blue) without gate metal. The red curve is almost overlapped by the blue curve. Inset: Enlargement of three curves near $V_d \sim 0$. (b) I_d-V_d curve and (c) transconductance relation of the in-plane GaAs NW MOSFET. Inset of (c): transconductance curve in semi-log scale. (d) $|I_g|$-V_g curve.

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